ET 438b Sequential Control and Data Acquisition

Department of Technology

LESSON 4: ON/OFF CONTROL APPLICATIONS AND DESIGNS

LEARNING OBJECTIVES

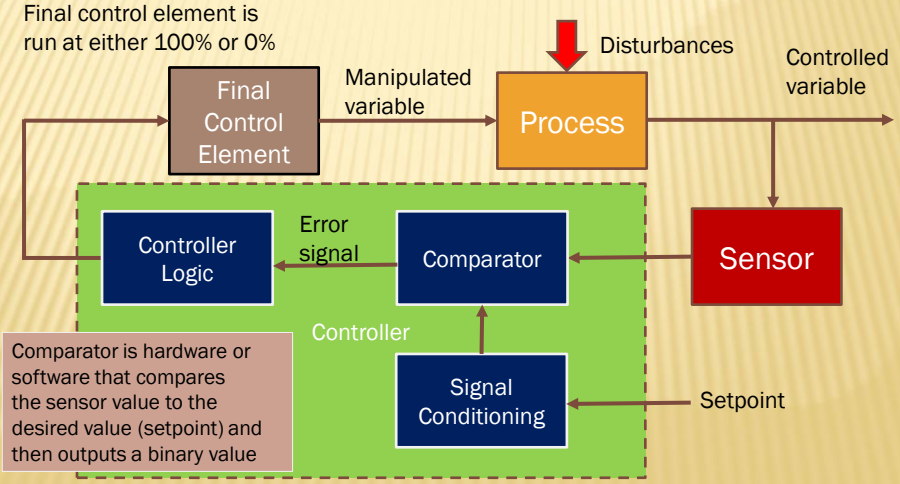
After completing this lesson you will be

- Explain the operation of on/off controllers
- Explain how hysteresis improves stability of on/off controllers
- Design an on/off controller using a comparator with hysteresis

SIMPLE DIGITAL CONTROL
ON/OFF PROCESS CONTROL

In on/off control error signal is binary in nature.

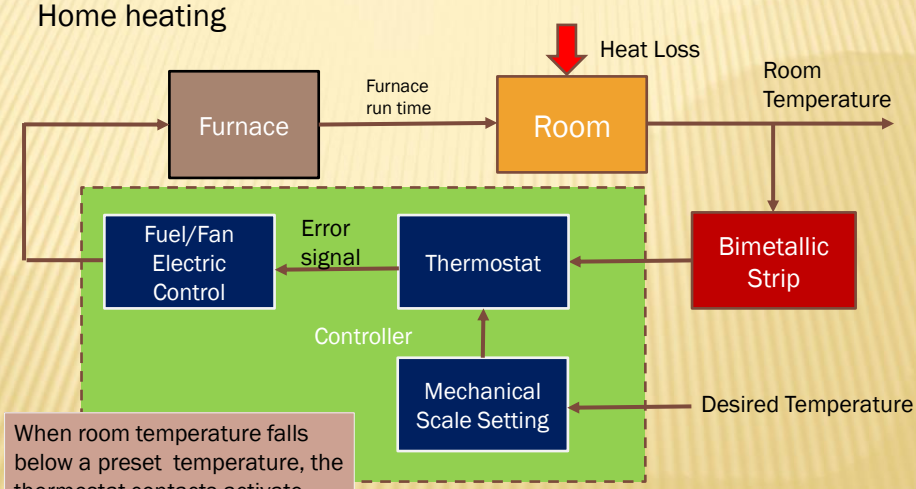
Final control element is run at either 100% or 0%



Comparator is hardware or software that compares the sensor value to the desired value (setpoint) and then outputs a binary value

ON/OFF CONTROL EXAMPLE

Home heating



When room temperature falls below a preset temperature, the thermostat contacts activate the furnace fan and fuel supply.

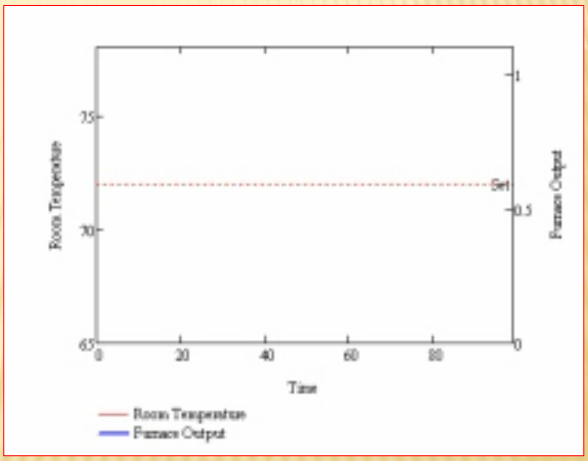
ON/OFF CONTROL APPLICATION CRITERIA

1. Precise control must not be required
2. Process must have sufficient internal storage capacity to allow final control element to supply the load while measurement is taken.
3. Energy entering the load must be small compared to the stored energy in the process

ON/OFF CONTROLLER TIME PLOTS

Controller output goes to 100% when the temperature falls below set point value .

Example for furnace shows furnace on when temperature falls below set point of 72 degrees



DIFFERENTIAL GAP CONTROLLER

To improve the stability of an on/off controller a hysteresis is added to the comparator element This is called differential gap control

Logic - when measured variable goes above upper boundary final control element turns on. Remains on until variable falls below lower level Gap also known as dead zone. Typically 0.5-2.0% of full range.

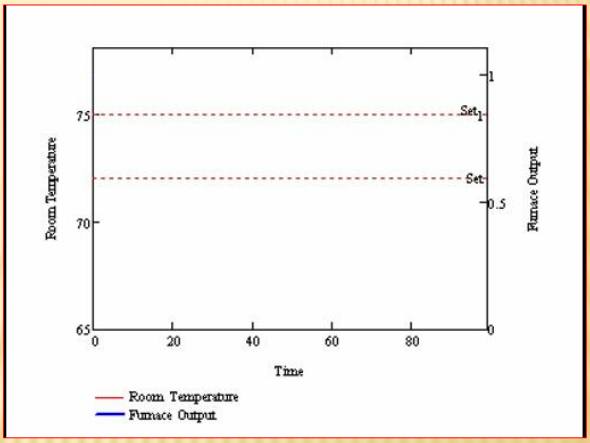
Gap introduces a known control error but reduces cycling

DIFFERENTIAL GAP CONTROLLER TIME PLOT

Furnace controller with 3 degree differential gap

Temperature below Set=72 degrees furnace on. Shut off temperature is Set_1=75 degrees.

Output depends on temperature and previous output state



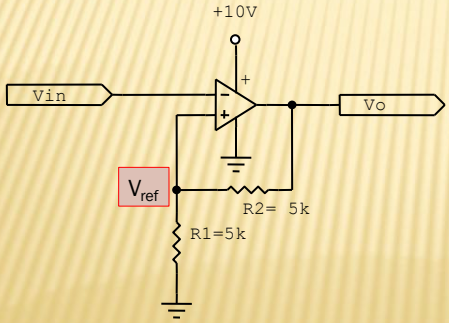
Controller Logic: IF Room Temp ≤ Set AND Furnace Output= 0 THEN Furnace Output =1 (T ↑)
IF Room Temp ≤ Set_1 AND Furnace Output= 1 THEN Furnace Output =0 (T↓)

COMPARATORS WITH HYSTERESIS

Implementing Differential Gap Control with Comparators requires hysteresis

Hysteresis - the output depends on the input and the previous state of the output.

Inverting Comparator with Hysteresis



Analysis: assume that $V_{in} < V_{ref}$

$V_0 = 0.8V_{cc}$

$V_o = +V_{sat} = 8$ Vdc

Determine V_{ref} from voltage divider formula

$$V_{ref} = V_o\left(\frac{R_2}{R_1 + R_2}\right)$$

$$V_{ref} = 8\left(\frac{5k}{5k + 5k}\right) = 4 \text{ Vdc}$$

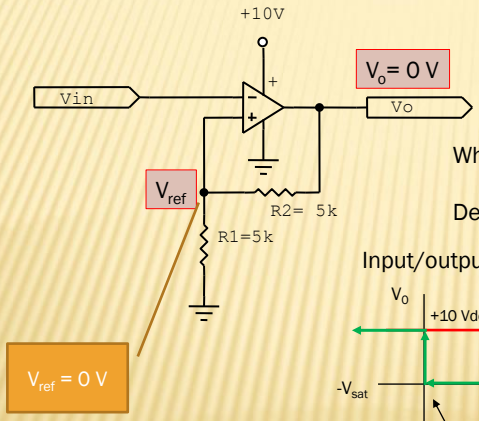
Define this as the upper trip point (UTP)

COMPARATORS WITH HYSTERESIS

Analysis continued

Now assume that $V_{in} > V_{ref}$

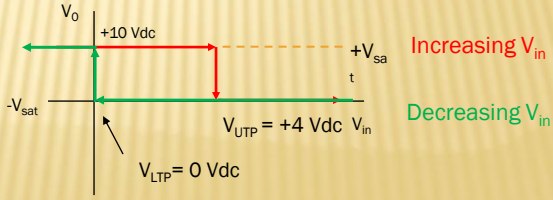
If $V_{in} > V_{ref}$, then $V_0 = -V_{sat} = 0$ Vdc



When $V_{in} > 0$, $V_o = 0$ Vdc and $V_{ref} = 0$ Vdc

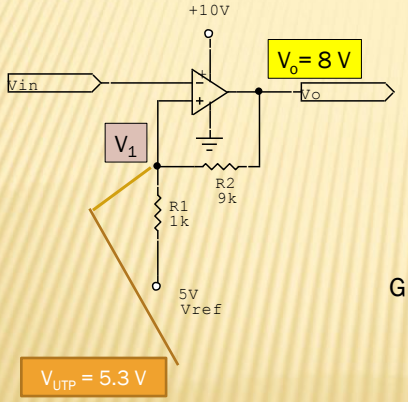
Define as lower trip point (LTP)

Input/output Plot Comparator with Hysteresis



COMPARATORS WITH HYSTERESIS

Non-zero voltage reference



Circuit Analysis

Use superposition to find the contributions to V_1 from output V_o and V_{ref}.

Assume $V_{in} < V_1$ $V_0 = +V_{sat} = 8$ Vdc

Ground V_{ref} and find contribution to V_1 due to V_o

$$V'_1 = V_o\left(\frac{R_1}{R_1+R_2}\right) = 8\left(\frac{1k}{1k+9k}\right) = 0.8\ V$$

Ground V_0 and find contribution due to V_{ref}

$$V''_1 = V_{ref}\left(\frac{R_2}{R_1+R_2}\right) = 5\left(\frac{9k}{1k+9k}\right) = 4.5\ V$$

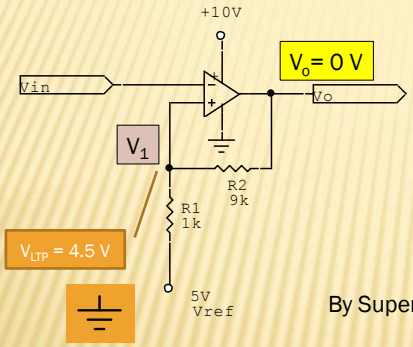
Final value when $V_{in} > V_1$

$$V''_1 + V'_1 = V_1$$
$$4.5 + 0.8 = 5.3\ \text{Vdc}$$

Upper trip point value (UTP)

COMPARATOR WITH HYSTERESIS - ANALYSIS

Non-zero voltage reference



Assume that $V_{in} > V_1$ so $V_0 = -V_{sat} = 0$ V

Since $V_o = 0$ and V_{ref} is grounded

$$V'_1 = V_0\left(\frac{R_1}{R_1+R_2}\right) = 0\ \text{Vdc}$$

Now find contribution due to V_{ref}

$$V''_1 = V_{ref}\left(\frac{R_2}{R_1+R_2}\right) = 5\left(\frac{9k}{1k+9k}\right) = 4.5\ \text{Vdc}$$

By Superposition

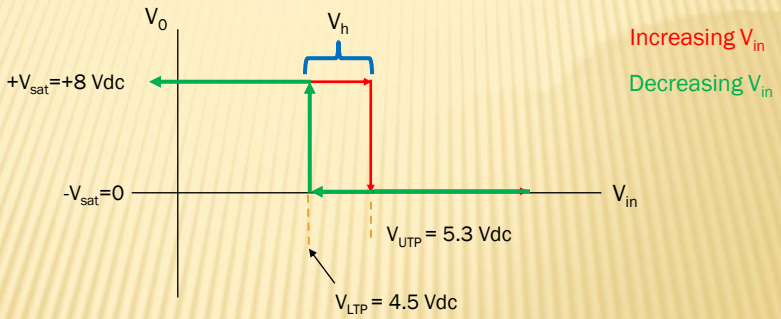
$$V''_1 + V'_1 = V_1$$
$$4.5 + 0 = 4.5\ \text{Vdc}$$

Lower trip point value (LTP)

Hysteresis voltage is the difference between the V_{UTP} and V_{LTP}. In this case: 5.3 - 4.5 = 0.8 Vdc (hysteresis)

COMPARATOR WITH HYSTERESIS - ANALYSIS

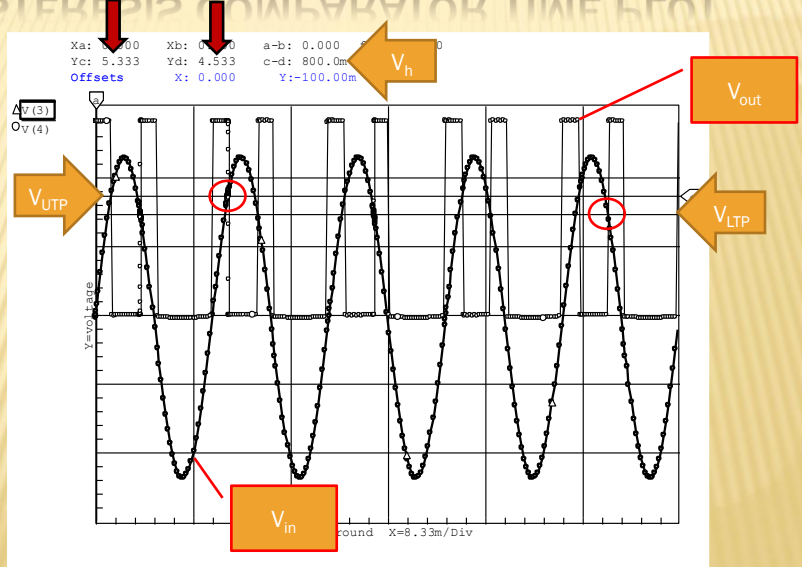
Input/output Plot



Hysteresis voltage is the difference between the V_{utp} and V_{ltp}.
In this case: 5.3 - 4.5 = 0.8 Vdc (hysteresis)

$$V_h = V_{UTP} - V_{LTP}$$

HYSTERESIS COMPARATOR TIME PLOT



COMPARATORS WITH HYSTERESIS

Design Equations and Procedure

Assumes bipolar output voltage

$$V_{UTP} = +V_{sat} \cdot \left[\frac{R1}{R1+R2}\right] + V_{ref} \cdot \left[\frac{R2}{R1+R2}\right] \quad 1$$

$$V_{LTP} = -V_{sat} \cdot \left[\frac{R1}{R1+R2}\right] + V_{ref} \cdot \left[\frac{R2}{R1+R2}\right] \quad 2$$

$$V_h = 2 \cdot V_{sat} \cdot \left[\frac{R1}{R1+R2}\right] \quad 3$$

Design Procedure

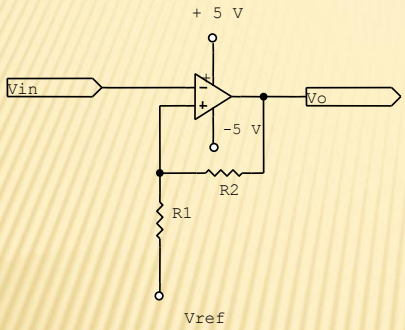
Given: V_{cc}, V_h, V_{UTP}, and R1,

1.) Find V_{sat}
2.) Use Equation 3 to find R2
3.) Use Equation 1 to find V_{ref}

DESIGN EXAMPLE

A temperature sensor has a gain of 20 mV/F. It will be used in an electronic thermostat system. Design a comparator with hysteresis circuit that will give a 4 degree F deadband for the thermostat control around a setpoint temperature of 72 degrees F. The comparator will use bipolar power supplies at +- 5Vdc. Interface the thermostat logic to a transistor driver (2N3904 h_{fe} = 300) that will actuate a furnace control relay. The relay has a dc resistance of 250 ohms.

DESIGN CALCULATIONS



Find Setpoint Voltage

$V_{sp} = (20mV/^{o}F)(72^{o}F) = 1.44V$

Find hysteresis Voltage from Temperature

$V_h = (0.020V/^{o}F)(4^{o}F) = 0.080V$

Inverting comparator so:

for $V_{in} > V_1$ $V_o = -V_{sat} = -5\ Vdc$

for $V_{in} < V_1$ $V_o = +V_{sat} = +5\ Vdc$

$$V_h = 2\,V_{sat}\left[\frac{R1}{R1+R2}\right] \quad \text{where } V_h = 0.080V,\ V_{sat} = 5V$$

DESIGN CALCULATIONS

Continued -1-

Substitute known values into above

$$0.080 = 2(5)\left[\frac{R_1}{R_1+R_2}\right] \Rightarrow 0.080\left[R1+R2\right] = 10R1$$

$0.08R2 = 9.92R1$

$R2 = \frac{9.92R1}{0.08} \Rightarrow R2 = 124R1$

Pick value of R1 and find R2

Let $R1 = 4.7K\Omega$

$R2 = 124(4.7K\Omega) = 582.8K\Omega$ NON-standard value

use standard value and potentiometer

DESIGN CALCULATIONS

Continued -2-

Set $V_{ref} = V_{sp}$ compute V_{LTP} and V_{UTP}

$$V_{UTP} = 5V\left[\frac{4.7k\Omega}{4.7k\Omega + 582.8k\Omega}\right] + 1.44\left[\frac{582.8k\Omega}{4.7k\Omega + 582.8k\Omega}\right]$$

$$V_{UTP} = 0.0963 + 1.4285V = 1.4688V$$

$$V_{LTP} = -5\left[\frac{4.7k\Omega}{4.7k\Omega + 582.8k\Omega}\right] + 1.44\left[\frac{582.8k\Omega}{4.7k\Omega + 582.8k\Omega}\right]$$

$$V_{LTP} = -0.040 + 1.4285 = 1.3885V$$

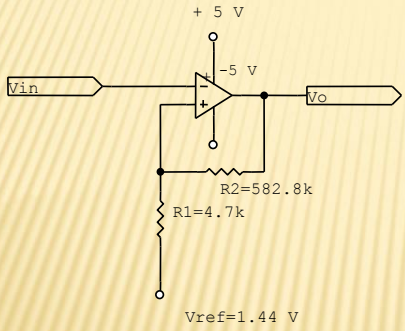
Check Centering

$$V_{UTP} - V_{ref} = 1.4688 - 1.4400 = 0.0288 = 28.8mV$$

$$V_{ref} - V_{LTP} = 1.44 - 1.3885 = 0.0515V = 51.5mV$$

DESIGN CALCULATIONS

Continued -3-



Convert V_{UTP} and V_{LTP} to °F

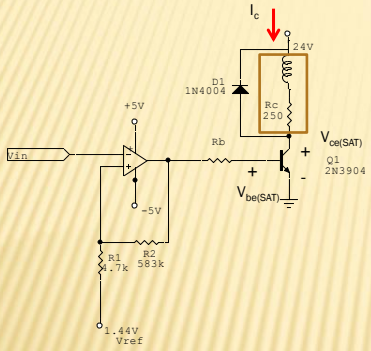
upper F set $\frac{1.4688V}{0.020V/°F} = 73.44°F$

lower F set $\frac{1.3885}{0.020V/°F} = 69.43°F$

Now include the transistor output stage

DESIGN CALCULATIONS

Find value of R_b to activate relay



Size resistor R_b so that Q_1 saturates

Assume saturation $V_{ce(SAT)} = 0.2V$, $V_{be(SAT)} = 0.8V$

Check output logic

When $V_{in} < 1.3885$ V, $V_o = +5$ Vdc (69.93 F)

FURNACE ON

When $V_{in} > 1.4688$V $V_o = -5$Vdc (73.44 F)

FURNACE OFF

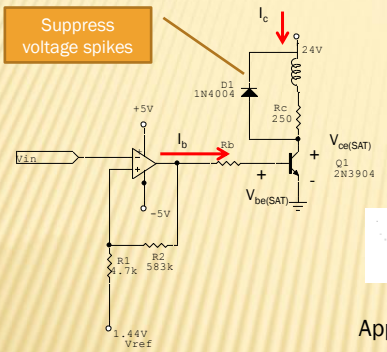
Find I_c assuming saturation

$$-24V + I_c R_c + V_{ce} = 0 \Rightarrow I_c = \frac{24 - V_{ce(SAT)}}{R_c}$$

$$I_c = \frac{24 - 0.2V}{250\Omega} = 95.2mA$$

DESIGN CALCULATIONS

Suppress voltage spikes



Relate I_c to I_b through h_{FE} (also known as β, dc current gain)

$$h_{FE} = 300 = \frac{I_c}{I_b}$$

Reduce h_{FE} by a factor of 10 due to effects of saturation on dc gain

$$I_b = \frac{I_c}{h_{FE}/10} \qquad I_b = \frac{95.2mA}{300/10} = 3.17mA$$

Apply KVL around the base-to-emitter circuit

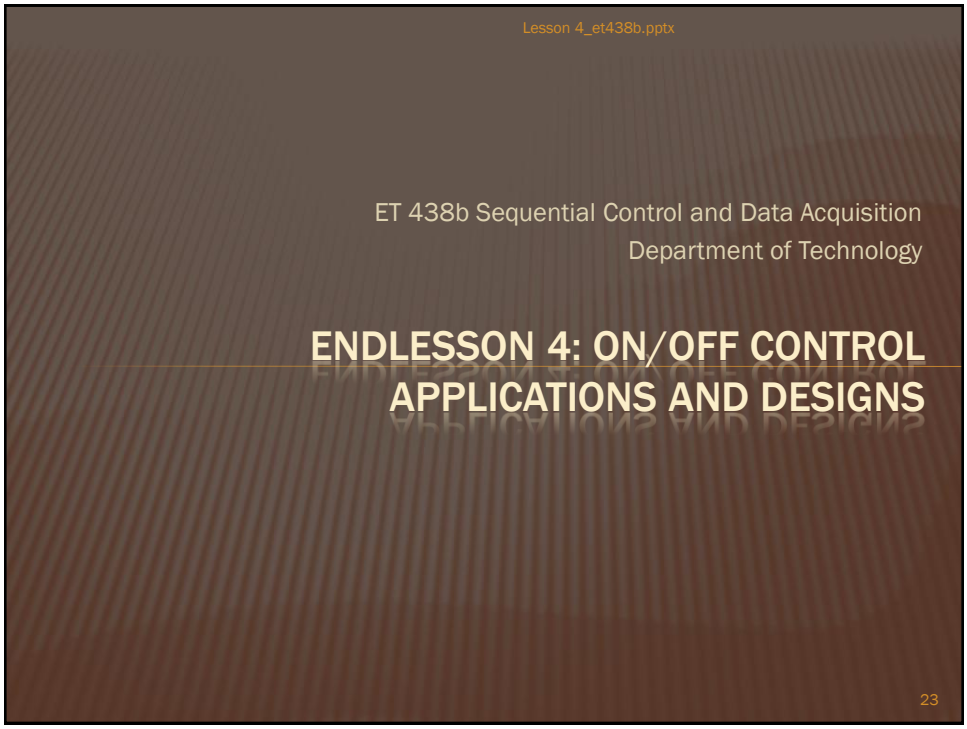
$$-V_o + I_b R_b + V_{be(SAT)} = 0$$

$$\frac{V_o - V_{be(SAT)}}{I_b} = R_b \qquad V_{be(SAT)} = 0.8V$$

When $V_o = -5$ Vdc Q1 base-to-emitter junction reverse-biased. Q1 cutoff

When $V_o = +5$ Vdc

$$\frac{5 - 0.8V}{3.17mA} = 1.325K\Omega$$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